READOUT ELECTRONICS FOR THE NA48 LIQUID KRYPTON CALORIMETER

- Overview
- Preamplifier
- Transceiver
- Shaper
- Digitization
- Data Flow
- Compactification
- Performance
- Implementation

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Orsay-Perugia-Pisa-Saclay-Siegen-Torino-Vienna-Warsaw
OVERVIEW

NA48 has proposed to measure the direct CP violation parameter $\epsilon'/\epsilon$ with an accuracy of $2 \times 10^{-4}$

$$Rp(\epsilon'/\epsilon) \simeq \frac{1}{6} \left( 1 - \frac{\Gamma(K_S^0 \rightarrow \pi^0 \pi^0)}{\Gamma(K_S^0 \rightarrow \pi^0 \pi^0)} \times \frac{\Gamma(K_S^0 \rightarrow \pi^+ \pi^-)}{\Gamma(K_L^0 \rightarrow \pi^+ \pi^-)} \right)$$

The neutral decays are reconstructed with the signals from a quasi-homogeneous calorimeter with liquid Krypton. It has about 13500 channels and was designed to reach an energy resolution

$$\frac{\sigma(E)}{E} = \frac{3.0\%}{\sqrt{E}} \oplus 0.50\% \oplus \frac{40 MeV}{E}$$

The readout electronics provides a dynamic range from a few MeV to about 50 GeV energy deposition per cell $\rightarrow K^0$ energies between 70 and 170 GeV

By shaping the calorimeter signals, sampling at 40 MHz and having 13,500 longitudinal cells it is possible to cope with the high rate of incident particles of about 1 MHz
Collect ionization charge signal and produce a voltage

Mounted inside the liquid Krypton (120°K) to minimize charge transfer time and noise (100 mW for 14,000 ch)

Integration time constant 150 ns. Total detector capacitance about 200 pF per cell
Figure 3: Calibration circuit.
Make pole-0 cancellation (change $\tau = 150$ ns into $\tau = 20$ ns) to decrease the risetime of the signal.

Make a differential output signal to the shaper that sits about 10 m away. Improve the common mode rejection and decrease the induction of coherent noise.
Make the signal narrow to increase rate capability. Delay the signal to allow for simultaneous determination of the gain for subsequent amplification.

1 differentiation followed by a 9-pole Bessel filter (9 integrations) producing a pulse delayed by 50 ns with 40 ns rise time, 73 ns FWHM and 160 ns at baseline, followed by a reasonably flat undershoot over 2.8 $\mu$s that is 3% of the pulse amplitude.

Shaper is an ASIC (1.2 $\mu$m BiCMOS) with external (1%) components to determine the filter characteristics.
Gain Switching Amplifier NA48 KRYPTON

Energy Ranges (GeV)

Input Voltage (V)

Digital Code
Slope Ratios

91/90

92/91

93/92

- Distributions cover ~ all channels of the calorimeter

- Individual gains stable to \( \leq 0.1\% \)

\( \leq 1\% \) spread
Gain Switching Amplifier NA48 KRYPTON

ADC resolution 8.8\text{ eff.\,bits}
\frac{1.5\text{MeV} \oplus 1.5\% \sqrt{E} \oplus 0.25\% E}{\text{rel gains}}
DIGITIZATION

Output signal of the shaper if amplified in a passive network with four different gains

Gain to be selected is determined concurrent with the shaping by comparing a copy of the differentiated shaper input signal with three programmable thresholds

Every clock cycle (25 ns) a gain can be selected. The lowest gain reached for a given input signal can be frozen for a programmable number of subsequent samples

To the selected gain stage output a programmable offset is applied that allows to avoid underflow for pileup signals

Gain switching thresholds, offsets and gain hold time are programmed via 6-bit DAC registers

The amplified shaper output is sampled in a 10-bit 40 MHz FADC (Philips TDA8760)

Modules were built that combine the shaper, FADC and sample buffering for 64 channels: Calorimeter Pipeline Digitizer (CPD)
7x7 cells with 100 GeV shower
7x7 cells with 100 GeV shower
7x7 cells with 100 GeV shower

GAIN INDEX

GAIN RANGE 3
GAIN RANGE 2
GAIN RANGE 1
7x7 cells with 100 GeV shower
CPDAS = DUAL-CHANNEL DAUGHTER CARD, ONE ON EACH FACE, WITH SHAPER, GAIN SELECTION, FADC AND BUFFER MEMORY ON EACH SIDE

CPD = MODULE HOLDING 32 CPDAS AND CONTROL CARDS (1 MB, 1 FASTBUS INTERFACE, 1 ADDRESS CONTROLLER, 1 TRIGGER SUM CARD)
DATA FLOW

Pairs of 12-bit words (10-bit FADC sample + 2-bit gain index) are written into a 8Kx12 \equiv (204.8 \mu s) circular buffer

Digitization is driven by a 40 MHz clock signal that is common to all detectors in the experiment.

Second level trigger \equiv timestamp \equiv circular buffer address \rightarrow copy ten 12-bit words (samples) for each channel into a linear buffer

From the linear buffer the samples are copied into a 9-stage digital pipeline that performs funneling and zero-suppression (compactification)
COMPACTIFICATION

Read shower box of 11x11 cells (91% of incident photon energy)

about 700 cells read for a neutral trigger event
about 150 cells read for a charged event

![Shower Profile]

- Suppressing individual channels and adding on lost tails of a cluster later through a fit profile is not optimal for getting a good energy resolution.

Better is to perform a halo expansion around hit cells.

16 channels hit array

Diamond:
(N|E|S|W) ⇒ Mark cell

Octagon:
(N&E)(S&E)(N&W)(S&W) ⇒ Mark cell

- Built 1024 ASIC's, each handling 16 calorimeter channels
Load Balancing at Output of Compactification
ANALOG PERFORMANCE

Baseline signal width about 160 ns

Time resolution about 300 ps (2.20 ps measured)
(100 ps electronics alone) (in 1997 !)

Overall incoherent noise:
2.8 ADC counts/ch =
2.3 ( PA) ⊕ 1.0 ( TX) ⊕ 1.2 ( CPD)

Overall coherent noise:
0.15 ADC counts/ch, while 0.075 for CPD alone
The overall coherent noise is a function of the location of the shower box in the calorimeter

Integral non-linearity over the working range of 300 - 950 ADC counts is less than 0.1%

Gains and gain ratio's stable to ≤ 0.1 %

28 dead preamps

replaced ~30 CPDAS
DIGITAL PERFORMANCE

- each pipeline stage is \( < 100 \, \mu\text{sec} \rightarrow \) sustained trigger rate of 10 KHz can be handled

- Current system can output \( 80 \, \text{MB/sec} \) to the event builder

- In 1998 output bandwidth will be 2-4 times larger after event builder upgrade

- During 1997 data taking period the average trigger rate was 5 kHz  
  event size was 9 KB (calorimeter alone)  
  throughput 40 MB/s

- Accelerator produces a burst of 2.5 sec every 14.4 sec
IMPLEMENTATION

13,212 preamplifiers (PA) mounted inside the liquid Krypton (122ºK)

13,212 transceivers (TX) mounted outside on the Krypton vessel

216 shaping & digitization (CPD) modules housed in 30 FASTBUS crates (per crate 330A at 5.2V and 95A at -5V) FASTBUS crates are chained using custom built Cluster Interconnect modules that provide galvanic isolation and signal synchronization with the experimental clock

32 Data Concentrator (DC) compactification modules in 2 custom crates with FASTBUS mechanics. DC crates are interconnected by custom built modules (DCI)

16 CES RIO8260 RISC processor boards (DRIO) for fan-in and event formatting in 8 VME crates

1 RIO8260 RISC processor (TIC) and 1 FIC8234 processor (SBC) in VME for fast and slow control

8 optical links to the event builder
Cost:

<table>
<thead>
<tr>
<th>item</th>
<th>KCHF</th>
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</thead>
<tbody>
<tr>
<td>PA</td>
<td>1000   incl cables, connectors, calibration system</td>
</tr>
<tr>
<td>TX</td>
<td>200    12 CHF per channel</td>
</tr>
<tr>
<td>CPD</td>
<td>3000   500 FADC, 400 ASIC, 1300 production, ...</td>
</tr>
<tr>
<td>DC</td>
<td>1000   1.41 CHF/channel 0-suppression ASIC</td>
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<tr>
<td>RIO</td>
<td>200</td>
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Summary

- **NA48** has a **working calorimeter readout based on a digital pipeline**

- **Dynamic range** is currently
  - 9 MeV - 60 GeV of deposited energy per cell (improved in 1998)

- The **electronics noise** is low (~9 MeV/keV) (improved in 1998)

- The **pulse shape** allows high incident rate

- The **readout bandwidth** is currently
  - 80 MB/s (improved in 1998)

- **$\phi$-suppression** via halo expansion works