The Design and Performance of the KTEV CSI Readout Electronics

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- Requirements
- Design
- Calibration
- Performance
- Reliability
- Conclusion
KTeV Calorimeter Requirements

KTeV calorimeter specs - 1% Energy resolution for a 15GeV photon
- 1mm position resolution for a 15GeV photon

3100 CsI CRYSTALS

See talk by Aaron Rodman

Readout Requirement

- Wide Dynamic Range
  - 16 Bits Dynamic Range
- Excellent Resolution
  - Better than 8 Bits Resolution
- Low Noise Performance
  - Differential Input Noise levels ~3fC
- Extremely Linear Response
  - Less than 0.1% non-linearity over the entire dynamic range
- Excellent Timing Resolution to Reject Accidentals
  - Deadtimeless Integration over an 18.9ns period (53MHz)
- Buffer the event until Level 1 Decision (~800ns)
- Buffer the event until Level 2 Decision (~2μs)
KTEV CSI Read Out System

- **Charge-Integrating**
- **Multi-Ranging**
  \[ \rightarrow 8\text{-Bit Mantissa} \]
  \[ \rightarrow 3\text{-Bit Exponent} \]
  \[ \rightarrow 16\text{-Bit Dynamic Range} \]
- **Pipelined (i.e. Deadtimeless) Operation**

System based on the Fermilab "Pie" Chip

- Originally intended for SSC use
- Now also adopted by CDF Upgrade and CMS

Concept: Bill Foster

Development led by: Robert Tschirhart

Ray Yarema
KTeV Calorimeter Readout System

- HV divider for the PMT bases
  - Hamamatsu PMTs (5 stage .75" R5364; 6 stage 1.5" R5330)
- The digital photomultiplier tube (DPMT) board
  - Charge Integrating and Encoding (QIE) ASIC
  - 8-bit Harris (HI1386) FADC
  - Driver Buffer and Clocking (DBC) ASIC
  - Read out into VME-based buffer (Pipeline)
QIE Operation

Current Splitter

Anode

I

I/2

I/4

I/8

I/16

I/32

I/64

I/128

I/256

C1  C2  C3  C4

4 capacitor ring buffer

FADC

(8 bit)

3-bit Range ID

(1 pf caps)

Clocked at 53MHz

4 capacitors x 8 ranges x 2 constants (offset + slope) = 64 constants
The Charge Integrating and Encoding (QIE*) ASIC

Features of the QIE

- 8 binary-weighted ranges (1/2 --> 1/256)
- Pipelined operation (integrate, encode, MUX, reset)
  - 4 capacitors/range --> continuous pulse shape integration
- Differential input for common mode noise rejection
- Differential analog and digital output
  - 2-bit CapID + 3-bit exponent + analog voltage

![Figure: FADC response versus input charge for 1st in-time integration period](image)

* The QIE was developed by T. Zimmerman and M. Sarraj (FNAL)
**QIE Dynamic Range**

Table: QIE response to input charge and the corresponding contribution to the resolution

<table>
<thead>
<tr>
<th>Range</th>
<th>Q_{input}</th>
<th>Resolution</th>
<th>Energy (GeV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/2</td>
<td>0-2pC</td>
<td>- 1.1%</td>
<td>0-0.2</td>
</tr>
<tr>
<td>I/4</td>
<td>2-6pC</td>
<td>0.3-0.1%</td>
<td>0.2-0.6</td>
</tr>
<tr>
<td>I/8</td>
<td>6-14pC</td>
<td>0.2-0.1%</td>
<td>0.6-1.4</td>
</tr>
<tr>
<td>I/16</td>
<td>14-30pC</td>
<td>0.2-0.1%</td>
<td>1.4-3.0</td>
</tr>
<tr>
<td>I/32</td>
<td>30-62pC</td>
<td>0.2-0.1%</td>
<td>3.0-6.2</td>
</tr>
<tr>
<td>I/64</td>
<td>62-126pC</td>
<td>0.2-0.1%</td>
<td>6.2-12.6</td>
</tr>
<tr>
<td>I/128</td>
<td>126-254pC</td>
<td>0.2-0.1%</td>
<td>12.6-25.4</td>
</tr>
<tr>
<td>I/256</td>
<td>254-510pC</td>
<td>0.2-0.1%</td>
<td>25.4-51.0</td>
</tr>
</tbody>
</table>

**FIGURE:** Fractional charge per RF cycle at 53MHz for a 175pC pulse.
The Driver/Buffer/Clocking (DBC*) ASIC

- **Functions of the DBC**
  - Terminate and synchronize 53MHz data from the QIE (exponent and CapID) & FADC (mantissa)
  - Provide a programmable phase trim for clocks to QIE & FADC
  - Continuously buffer QIE & FADC data into a 40 slice FIFO until receipt of a Level-1 trigger
  - Buffer 32 slices of data into a 2nd FIFO until receipt of a Level-2 trigger
  - Upon receipt of Level-2, send data through a parallel to serial converter
  - Drive data on 4 parallel differential lines at 26MHz from DPMT to the Pipeline

* The DBC was developed by Jihad Srage (FNAL).
Production Issues

- **QIE and DBC production devices**
  - QIE & DBC fabricated on the same wafer using the Orbit 2.0 μm Bi-CMOS process
    - Up to ~20% gain (capacitance) differences between process runs for the QIE
    - Gain variation ~1-2% between QIEs from a process batch
    - Chips packaged into 64-pin thin quad flat pack (ASAT)
      - No degradation in device performance due to packaging
      - Devices can be quickly and easily replaced
      - Chips tested before board assembly (typically ~60% yield)*

- **DPMT board and HV divider are separate boards**
  - DPMT boards can be replaced quickly
  - Boards tested before calorimeter installation (typically ~75% yield)*
**CALIBRATION SCHEME**

Electronics Calibration

→ Extract 64 parameters for each QIE

C6I Calibration

→ Use momentum analyzed $\theta^\pm \ (K \rightarrow \pi^\pm e^\pm \nu)\$

To extract the block gains

→ See talk by Aaron Roosdman to see impressive results!
Laser Calibration and Monitoring

Purpose:
- Electronics Calibration
  - Extract 64 Parameters/Channel
- Monitor short-term PMT Gain Drifts
- Online Monitoring and Alarm

Design:
- F-Tripled 50 mJ/pulse Nd:Yag Laser
  - 355 nm to Excite Fluorescent Dye
    - High power to deliver up to $10^6$ RE/Channel
    - Good Time Jitter (< 0.5 nsec) + Power Stability
- Liquid Fluorescent Dye
  - Geometrically stable & Isotropic Light Source (very nice for distributing light to 3166 Channels)
    - Can be made laser damage-resistant
    - Fluorescence tuned to mimic CsI scintillation
- Pin Photodiode and 20-bit Q-ADC System
  - Linear + Stable Reference Basis for Calibration
  - No Amplifiers used
Light Distribution System
(ONE OF FOUR)

Primary Fiber

Dye in ➔

Secondary Fibers

out ➔

LED

Laser Dye

Cuvette

Photo Diodes

Not Shown
"2.5:1" nonlinearity of a PIN Photodiode

(Hamamatsu S1728-02, no amplifier)
Calorimeter Performance

- Typical pedestal RMS for a single capacitor is ~0.36 counts (3.6 fC)

- Cross-talk between channels on a rib was measured to be less than 0.1%

FIGURE: Pedestal RMS from the sum of 4 clock cycles for all 3100 channels of the KTeV CsI calorimeter.
DPMT Performance

- In-situ calibration using a YAG laser system
  - light is collected using PIN-diodes and digitized using a Burr-Brown 20-bit ADC (DDC101)
- Laser calibration scans performed ~2 times/week
  - Excellent tool for debugging problems in the array
- Fractional residuals are typically less than 0.2% over the full dynamic range

**FIGURE:** Deviations from expected response after linearizing the output of the DPMT output. Residuals plotted are from the same laser data from which constants were derived.
DPMT Performance

- Electronic calibration is extremely stable
  - RMS residual for 3100 channels using 1 week old constants.

*FIGURE:* RMS residual of calorimeter electronics when calibrated with constants derived from 1 week old data.
DPMT Performance

- DPMT has excellent timing resolution

  - Timing resolution studies using laser data show a better than 150ps resolution

FIGURE: Timing resolution measured using laser data.
System Reliability

QIE and DBC chips suffered serious Orbit Process Problems:

\{(1) Voids developed in metal-1 layer which then took on fuse-like behavior (fatal for high current density areas) \\
(2) DBC mask flaws (genetic defect)\}

Manifetations:

\{(1) Increasingly poorer calibration \\
(2) Hard Failures (1-3 per day)\}

Some Consequences:

\{(1) 3 rounds of array-wide chip replacements + refab. \\
(2) For '96 data, clock speed = 53 MHz/3 (instead of 53) to reduce current density in DBC. \\
(3) 50% individual DMT channel swaps during production running \\
   (required steering beam away for access)\}
Conclusions

- **Inspite of serious flaws, KTeV '96-'97 run was quite successful due to:**
  - Superb online monitoring
  - Ease of replacement (10 mins./channel)

- Problems stem from process control, not design flaws.

- Successful application of QIE technology:
  - Possible to calibrate device and achieve high resolution
  - Modified version of QIE for CDF CAL. UPGRADE
  - CMS/HCAL has adopted QIE